Micronas.7397

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|---|
| **APPLICANT:** | Czech et al. | **GROUP:** | 2826 |
| **SERIAL NO:** | 10/761,144 | **EXAMINER:** | Tan N. Tran |
| **FILED:** | January 20, 2004 | | |
| **FOR:** | VOLTAGE COUPLING CIRCUIT FOR AN INTEGRATED CIRCUIT | | |

**Mail Stop Issue Fee**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

## TRANSMITTAL OF FORMAL DRAWINGS

Applicant submits herewith formal drawing(s) for this application. Attached please find four **(4)** sheets of formal drawings for this application.

The three month period of response set in the Notice of Allowability (PTOL 37) expires on **January 23, 2007** and this submission is on or before this expiry date.

Respectfully submitted,

Patrick O'Shea

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kim M. Hume

12/04/06
Date